Silicon synapses self-correct for both mismatch and design inhomogeneities

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A neuromorphic chip with an array of neurons has connections ("synapses") which implement a biological learning mechanism known as spike-timing-dependent plasticity ("STDP"). STDP is a homeostatic mechanism which regulates the firing rate of neurons. This mechanism is shown here to reduce variation in performance between neurons, due to both mismatch in fabrication and inhomogeneities in the electronic design.

*Introduction:*Neuromorphic engineers create integrated circuits which mimic neural computation in biological nervous systems. This may have applications in real-time, low-power, mobile processing, particularly in neural prosthetic devices. In a typical neural chip, analogue circuits model the electrical behaviour of nerve cells, with currents through transistors physically representing currents through nervous membranes [1]. Mismatch results in variation in the excitability of integrated neurons. Although this can be representative of the variation between biological neurons, it is not always desirable. One way to compensate for this variability is calibration through programmable neural network wiring [2]. However, in the connections between biological neurons ("synapses"), there is a learning mechanism in which the relative timing of spikes (the electrical pulses with which neurons communicate) from neurons before and after a synapse causes changes in synaptic strength [3]. This spike-timing-dependent plasticity (STDP), as it is known, has interesting computational properties: it can detect correlations, with inputs to a neuron which have more correlated activity working together to strengthen their synapses at the expense of others which are weakened; also, when the spike rates of inputs to a neuron are raised, the strengths of its incoming synapses tend to reduce, providing negative feedback on the increase in the rate of spikes produced, [4]. Thus STDP is a form of homeostasis, one of many found in biological neural networks [5]. STDP can be used explicitly as an engineering solution to ameliorate the effects of mismatch in analogue computations [6]. Here STDP in its native context of a neuromorphic chip is shown to partially compensate for mismatch as well as design inhomogeneites.

*Methods:*In this work, a chip has been designed in order to investigate issues in developmental neuroscience [7]. Its silicon synapses implement STDP; the learning rule and the circuit used are fully described in [8]. To briefly describe the system, 32 neuron circuits are integrated on each chip, each neuron had 64 dedicated circuits for incoming synapses, and 8 chips were used together to create a grid of neurons. Spikes, represented as digital pulses, are received at synapse circuits and create currents in proportion to the strength of the synapse, which is stored as a voltage across a capacitor. These currents indirectly charge another capacitor representing the activation of the neuron, and the neuron may then produce digital spikes of its own. The spikes cause integration of charge on other capacitors and this short-term memory of spike arrival times is used to change the strengths of the synapses according to the learning mechanism.

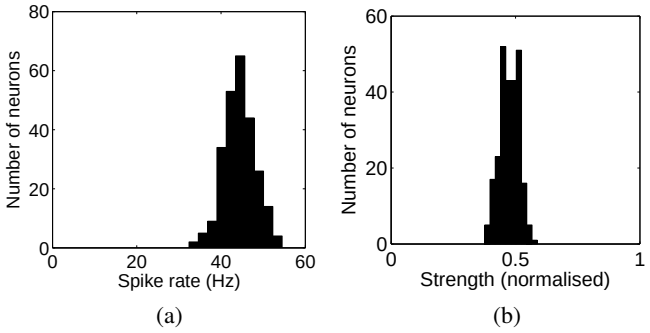

Fig. 1 *(a) Histogram of output spike rates for the neurons (mean rate: 44 Hz, std.dev. 3.8 Hz); (b) Histogram of mean strength of all the incoming synapses for each neuron (mean normalised strength: 0.48, std.dev. 0.039)*

At every stage there is variation in the performance of different neuron and synapse circuits, due to mismatch in integrated transistors and capacitors. To observe the effects of mismatch on the excitability of neurons, the synapses of each neuron were connected to the same set of inputs, and typical input was provided. Thus in a completely homogenous system with no mismatch, neurons should perform identically (excepting a small contribution of electronic noise). The input consisted of independent poisson spike trains (20 Hz); these were generated by a PC for a simulated set of input neurons, and randomly connected to the 64 input synapses of each on-chip neuron. The experiment lasted 10 s. Output spikes were streamed back to the PC to be counted. The strengths of synapses, represented as voltages, were sequentially sampled with a custom recording system immediately after the end of the experiment. These voltages were then converted into a normalised scale based on their maximum and minimum possible values. Pearson correlation coefficients were calculated, along with related one-tailed t-tests, for various groupings of the on-chip neurons.

*Results:*Within each neuron, the same synapse would receive the same spike almost simultaneously, as each spike is transmitted as a timed pulse on physical wires spanning each chip and reaching each synapse. During the experiment some neurons spiked more than others (fig. 1a); fig. 2(a) shows how these spike rates were distributed around the neurons. There are some broad differences between chips (inter-die variation) and some random variation between neurons within the same chip. There is also systematic variation within chips, with the right-most and left-most columns of neurons spiking less than the columns in the middle; this is the result of differences in the pulse lengths at each neuron, as pulses are broadcast laterally across the chip; this inhomogeneity could be engineered out with careful attention to the clock distribution network [9], at the expense of design simplicity. Also, the bottom-right neuron in every chip has a lower spike rate because some voltages in these neurons were buffered out for test purposes, but the buffers added capacitance to the neurons and affected their functioning; this inhomogeneity could be compensated with a more complex design.

During the experiment, the strengths of the synapses quickly reduced from their initial maximum level due to STDP, some more than others (fig. 1b). Fig. 2(b) gives the distribution of these weights around the neurons. There is an inverse relationship between the spike rate of a neuron and the mean weight of its synapses — those neurons which spiked faster ended up with more depressed synapses (the relationship is shown in fig. 2(c); it is significant). This is the homeostatic effect of STDP in action; weaker incoming synapses make the neuron less likely to fire, providing negative feedback on the divergence of spike rates, so the spread is not so great as it would be if not for STDP. Interestingly, this compensation worked not

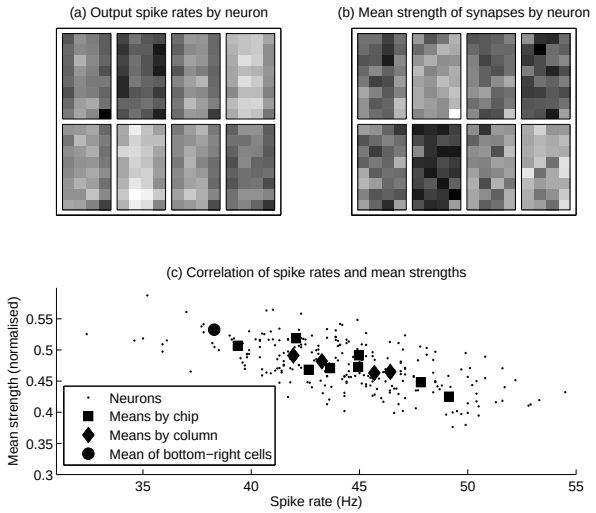

Fig. 2 *(a) Distribution of output spike rates across chips. Each raster cell is a neuron. White gaps show the boundaries between chips. Shading gives the output spike rate, white=fastest, black=slowest. (b) Distribution of mean strengths of synapses for neurons across chips: white=strongest, black=weakest. (c) Relationship of spike rates to mean strengths. Each data point represents a neuron. Pearson correlation coefficient (ρ) = -0.61 (this is significant: p=4.8×10^{-28}, n=256, one-tailed t-test). The mean of the cells with extra capacitance in the corner of each chip is shown; its location demonstrates compensation for low spike rate. Neurons are also grouped by chip, showing compensation for inter-die variation (ρ=-0.85, p=3.8×10^{-3}, n=8, one-tailed t-test), and by column, showing compensation for clock distribution inhomogeneity (ρ=-0.98, p=9.7×10^{-3}, n= 4, one-tailed t-test).*

just for random variation but also for the aforementioned inhomogeneities in electronic design. This is shown statistically for the variation between columns due to pulse lengths (fig. 2(c) caption) and graphically for the corner cells with added capacitance.

*Conclusion:*In a neuromorphic chip, STDP has acted to reduce variation in performance between neurons, due to both mismatch in fabrication and inhomogeneities in the electronic design. This type of learning is unsupervised and self-contained; it does not require calibration. It may prove fruitful for electronic engineers to investigate other neural homeostasis mechanisms.

References

1 M. Mahowald and R. Douglas, "A silicon neuron," *Nature*, vol. 354, pp. 515 – 518, 1991.

2 E. Neftci and G. Indiveri, "A device mismatch compensation method for VLSI neural networks," in *IEEE Biomedical Circuits and Systems Conference (BIOCAS)*, 2010.

3 L. Zhang, H. Tao, C. Holt, W. Harris, and M. Poo, "A critical window for cooperation and competition among developing retinotectal synapses," *Nature*, vol. 395, pp. 37–44, 1998.

4 S. Song, K. Miller, and L. Abbott, "Competitive Hebbian learning through spike-timing-dependent synaptic plasticity," *Nature*, vol. 3, pp. 919–926, Sept 2000.

5 G. Turrigiano, "Homeostatic signaling: the positive side of negative feedback," *Current Opinion in Neurobiology*, vol. 17, pp. 318–324, 2007.

6 K. Cameron, V. Boonsobhak, A. Murray, and D. Renshaw, "Spike Timing Dependent Plasticity (STDP) can ameliorate process variations in neuromorphic VLSI," *IEEE Transactions on Neural Networks*, vol. 16, pp. 1626–1637, 2005.

7 S. Bamford, A. Murray, and D. Willshaw, "Large developing receptive fields using a distributed and locally reprogrammable address-event receiver," *Neural Networks, IEEE Transactions on*, vol. 21, pp. 286–304, 2010.

8 S. Bamford, A. Murray, and D. Willshaw, "Spike-timing-dependent plasticity with weight dependence evoked from physical constraints," *IEEE Transactions on Biomedical Circuits and Systems*, 2012 in press; note to reviewers: this can be seen at: http://www.sim.me.uk/neural/JournalArticles/BamfordEtAl2012TBCAS.pdf.

9 G. Friedman, "Clock distribution networks in synchronous digital integrated circuits," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 665–692, 2001.